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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
08/942,333	10/01/97	NOURI A	MNFRAME.020A

LM02/0721
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EXAMINER	
TRAN, P	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 08/942,333	Applicant(s) Ahmad Nouri Et. Al.
	Examiner Philip B. Tran	Group Art Unit 2758

☒ Responsive to communication(s) filed on *Jun 14, 1999* .

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *three* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *1-30* is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-30* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐approved ☐disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____ .

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____ .

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). *8, 9, & 14*

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

1. Claims 12-30 are added. Therefore, claims 1-30 are presented for examination.

2. **The declaration under 37 CFR 1.131 is insufficient to overcome the rejections based on the Ote et. al. (reference).**

Applicant's Exhibits A-I, have no reference to the combined claimed feature, and fail to support Applicant's statement regarding the conception of the claimed invention prior to November 1995.

Regarding the date of **reduction to practice**, Applicant's Exhibits A-I provide no description of "a system for resetting a computer comprising a first computer; a microcontroller capable of providing a reset signal to the first computer; a remote interface connected to the microcontroller; and a second computer connected to the first computer via the remote interface and communicating a reset command to the microcontroller". No description of the claimed invention have been provided.

The current declaration is silent regarding the functionality and operability of managing, resetting and updating system status for a computer.

For all the reasons discussed above, the evidence submitted is insufficient to establish a reduction to practice of the invention in this country prior to the date of the Ote et. al. (reference).

Again, the evidence as a whole contains no sketches, blue prints, notes, records of meetings, etc. as proof that Ahmad Nouri and Karl Johnson are joint inventors regarding the conception of the claimed invention.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

4. Claims 1-2, 4-7, 10-13 and 16-19 are rejected under 35 U.S.C 102(e) as being anticipated by Ote et. al. (Hereafter, Ote), U.S. Pat. No.5,815,652.

Regarding claim 1, Ote teaches a system for resetting a computer comprising :

a first computer (i.e., computer to be managed **10**);

a microcontroller (i.e., agent **17**) capable of providing a reset signal (i.e., managing power on /off) to the first computer ;

a remote interface (i.e., SVP board **12** and asynchronous I/F **123** & **124**) connected to the microcontroller; and

a second computer (i.e., remote managing computer **27** or local managing computer **23**) connected to the first computer via the remote interface and communicating a reset command (i.e., controlling and managing power on/off remotely) to the microcontroller [see Figs. 23A & 23B and Abstract and Col. 12, Line 37 - Col. 13, Line 15 and Col. 13, Lines 40-67].

Regarding claim 2, Ote further teaches the system of claim 1 wherein the remote interface includes a power source independent of a power source for the first computer (i.e., power unit **13** controls power on/off of computer to be managed **10** while the SVC board and asynchronous I/F is supplied from the sub-power supply **131**) [see Figs. 5-23 and Col. 10, Lines 9-13].

Regarding claim 4, Ote further teaches the system defined in claim 1 wherein the second computer at the same location as the first computer (i.e., local managing computer **23** is in the same LAN (**22**) with the computer to be managed **10**) [see Figs 23A & 23B].

Regarding claim 5, Ote further teaches the system defined in claim 1 wherein the second computer is at a location remote to the first computer (i.e., remote managing computer **27** is at a location remote to the computer to be managed **10**) [see Figs 23A & 23B].

Regarding claim 6, Ote further teaches the system defined in claim 5, additionally comprising a pair of modems, wherein a first modem (i.e., modem **261**) connects to the first computer (i.e.,computer to be managed **10**) and a second modem (i.e., modem **262**) connects to the second computer (i.e., remote managing computer **27**) [see Figs 23A & 23B].

Regarding claim 7, Ote further teaches the system defined in claim 6 wherein each modem connects to the public switch telephone network (i.e., the user can enter the phone number to make a connection through the modem) [see Col. 6, Line 56 - Col. 7, Line 2].

Regarding claim 10, Ote further teaches the system defined in claim 1 wherein the remote interface includes a remote interface microcontroller that connects via a bus to the microcontroller [see Figs. 22 and 23A & 23B].

Regarding claim 11, Ote further teaches the system defined in claim 1 wherein the remote interface is responsive to a command sent from the second computer to reset the first computer [see Abstract and Col. 8, Lines 5-18 and Col. 12, Line 37 - Col. 13, Line 15].

Regarding claim 12, Ote further teaches the system defined in claim 1 wherein the computer includes a central processing unit (i.e., main unit CPU **52**) [see Fig. 22].

Regarding claim 13, Ote further teaches the system defined in claim 1 wherein the microcontroller is a general purpose microcontroller (i.e., one which is designed for multiple uses such as managing power control and monitoring fault of computer, etc.) [see Abstract and Col. 4, Lines 62-64].

Regarding claim 16, Ote further teaches the system defined in claim 1 wherein the remote interface is connected to and proximately located to the first computer (i.e., using SVP board **12**) [see Figs. 23A & 23B and Col. 4, Line 46 - Col. 5, Line 18 and Col. 12, Line 49 - Col. 13, Line 15].

Regarding claim 17, Ote further teaches the system defined in claim 2 wherein the independent power source powers the first computer when the first computer power source is inoperable or operating below a threshold power level (i.e., power-on request may be sent to the power control circuit of the SVP board to remotely turn on the power supply of the main unit) [see Col. 3, Lines 30-38].

Regarding claim 18, Ote further teaches the system defined in claim 1 wherein the remote interface is capable of communicating the results of the reset command to the second computer (i.e., sending fault logs and power status to the manager of the second computer through the SVP board) [see Col. 7, Line 18 - Col. 8, Line 4].

Regarding claim 19, Ote further teaches the system defined in claim 18 wherein the remote interface comprises a circuit having a remote interface microcontroller and a remote interface memory, and program code stored in the memory, and wherein the remote interface memory is connected to the remote interface microcontroller and stores the result data [see Fig. 22 and Col. 9, Line 61 - Col. 10, Line 67].

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 10 (c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 3, 8-9, 14-15 and 20-30 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Ote et. al. (Hereafter, Ote), U.S. Pat. No.5,815,652.

Regarding claim 3, Ote does not explicitly teach the remote interface includes an external port. However, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Ote by using external port for connection to the second computer. One would be motivated to do so to provide a channel for transferring data between the first and second computers.

Regarding claims 8-9, Ote does not explicitly teach the claimed limitation wherein each modem facilitates connection to the cable network or satellite. However, the concept and advantages of connecting a pair of modems through the cable network or satellite is well-known in the data communication network art. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Ote by specifying connection of a pair of modem through the cable network or satellite. One would be motivated to do so to provide a back up path of communication.

Regarding claims 14-15, Ote does not explicitly teach the system of claim 1 comprising a plurality of other microcontrollers and a microcontroller bus interconnecting the plurality of other microcontrollers and the microcontroller. However, it would have been obvious to one of ordinary skill in the art at the time of the invention to have combined additional microcontrollers and buses and put them into the system of Ote because doing so would make the system faster. As shown in "*St. Regis paper Co. v Bemis Co.*, 193 USPQ 8 (7th Cir. 1977)", to duplicate parts for multiple effects is generally not given patentable weight or would have been obvious improvements.

Regarding claim 20, Ote teaches a microcontroller network for diagnosing and managing the conditions of a computer comprising :

a computer including a central processing unit (i.e., main unit CPU **52**) [see Fig. 22]; and

a microcontroller (i.e., agent **17** manages the conditions of the computer to be managed **10** and resets (i.e., controls power on/off) the central processing unit or the computer to be managed **10**) [see Figs. 23A & 23B and Abstract and Col. 12, Line 37 - Col. 13, Line 15 and Col. 13, Lines 40-67].

Ote does not explicitly teach the system of claim 20 comprising a microcontroller bus and a plurality of microcontrollers that are interconnected by the microcontroller bus. However, it would have been obvious to one of ordinary skill in the art at the time of the invention to have combined additional microcontrollers and buses and put them into the system of Ote because doing so would make the system faster. As shown in "*St. Regis paper Co. v Bemis Co.*, 193 USPQ 8 (7th Cir. 1977)", to duplicate parts for multiple effects is generally not given patentable weight or would have been obvious improvements.

Regarding claim 21, Ote further teaches the system defined in claim 20 comprising a remote interface (i.e., SVP board **12** and asynchronous I/F **123** & **124**) wherein the remote interface comprises another selected one of the microcontrollers (i.e., SVP controller **121**) [see Figs. 22 and 23A & 23B].

Regarding claim 22, Ote further teaches the system defined in claim 21 wherein the remote interface includes a power source independent of a power source for the computer (i.e., power unit **13** controls power on/off of computer to be managed **10** while the SVC board and asynchronous I/F is supplied from the sub-power supply **131**) [see Figs. 5-23 and Col. 10, Lines 9-13].

Claim 23 is rejected under the same rationale set forth above to claim 20 except for the following limitation which is further taught by Ote :

a recovery manager (i.e., manager **241** or **242**) connected to the microcontroller bus, the recovery manager managing system status of the first computer (i.e., computer to be managed **10**) and sending a reset command to the central processing unit (i.e., monitoring the system status and controlling the power on/off of the computer to be managed **10**) [see Figs. 22-24 and Col. 11, Line 21 - Col. 13, Line 39].

Regarding claim 24, Ote further teaches the microcontroller network of claim 23 wherein the recovery manager (i.e., manager **241** or **242**) executes on a second computer (i.e., remote managing computer **27** or local managing computer **23**) [see Figs 23A & 23B].

Regarding claim 25, Ote further teaches the microcontroller network of claim 23 wherein the recovery manager includes a graphical user interface (i.e., using a graphic user interface as a means to manage and display information) capable of obtaining information utilized in sending the reset command [see Col. 7, Lines 18-47 and Col. 12, Line 48 - Col. 13, Line 15].

Regarding claim 26, Ote further teaches the microcontroller network in claim 23 wherein one of the microcontrollers is a remote interface microcontroller (i.e., SVP manager **29** of the remote managing computer **27**) [see Fig. 23B].

Regarding claim 27, Ote further teaches the microcontroller network of claim 26 wherein the remote interface microcontroller interconnects the microcontroller bus with the recovery manager (i.e., the manager **242** connects with the SVP manager **29**) [see Fig. 23B]. It is inherent that the connection is made via a bus.

Claim 28 is rejected under the same rationale set forth above to claim 22.

Regarding claim 29, Ote further teaches the microcontroller of claim 28 wherein the independent power source connected to the remote interface microcontroller provides power to the first computer when the first power supply fails (i.e., power-on request may be sent to the power control circuit of the SVP board to remotely turn on the power supply of the main unit) [see Col. 3, Lines 30-38].

Regarding claim 30, Ote further teaches the microcontroller network of claim 26 wherein the remote interface microcontroller is connected to and proximately located to the first computer (i.e., using SVP board **12**) [see Figs. 23A & 23B and Col. 4, Line 46 - Col. 5, Line 18 and Col. 12, Line 49 - Col. 13, Line 15].

7. Applicant's arguments with respect to claim 1-30 have been considered but are deemed to be moot in view of the new grounds of rejection.

Other References Cited

8. The following references cited by the examiner but not relied upon are considered pertinent to applicant's disclosure.

A) Giorgio, U.S. Pat. No. 5,761, 085 : Method for monitoring environmental parameters at network sites.

C) Heider, U.S. Pat. No. 5,276,863 : Computer system console.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Philip Tran whose telephone number is (703) 308-8767. The examiner can normally be reached on Monday through Friday from 8:00am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ahmad Matar, can be reached on (703) 305-4731.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

10. A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS ACTION IS SET TO EXPIRE **THREE** MONTHS, OR THIRTY DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION. FAILURE TO RESPOND WITHIN THE PERIOD FOR RESPONSE WILL CAUSE THE APPLICATION TO BECOME ABANDONED (35 U.S.C. § 133). EXTENSIONS OF TIME MAY BE OBTAINED UNDER THE PROVISIONS OF 37 CFR 1.136(A).

11. Any response to this action should be mailed to:

Commissioner of Patent and Trademarks

Washington, D.C. 20231

or faxed to : (703) 308-9051, (for formal communications intended for entry)

or: (703) 305-5356 (for informal or draft communications, please label "PROPOSED" or "DRAFT").

Hand-delivered responses should be brought to Crystal Park II,

2121 Crystal Drive

Arlington, VA., Sixth Floor (Receptionist).

PBT
Philip Tran
Art unit 2758
July 14,1999

AHMAD F. MATAR
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